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Notice of Allowability	Application No.	Applicant(s)	
	10/790,004	SHIH, PO-SHENG	
	Examiner	Art Unit	
	William C. Vesperman	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/2/2004*.

2. ☒ The allowed claim(s) is/are *14 - 26*.

3. ☒ The drawings filed on *02 March 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *10/367,756* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 4/2/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This action is in reply to applicant's filing of 3/2/2004.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Scott A. Mc Keown on August 4, 2004.

A. Please replace Claim 14, with revised Claim 14 as shown below.

14. A method comprising: fabricating an X-ray detector array, including the steps of:

providing a substrate having a capacitor area and a transistor area;

forming a gate line transversely extending on the substrate, wherein the gate line includes a gate electrode in the transistor area;

forming a gate insulation layer on the gate line, the gate electrode and the substrate;

forming a semiconducting layer on the gate insulation layer;

forming a first conductive layer on the semiconducting layer;

using a gray-tone photolithography, removing part of the first conductive layer and the semiconducting layer to form a common line longitudinally extending on a first semiconducting island, and a source electrode, a drain

electrode and a longitudinally extending data line on a second semiconducting island thereby forming a thin film transistor (TFT) structure, wherein the drain electrode electrically connects the data line;

forming a second conductive layer on the gate insulation layer in the capacitor area and to cover the common line;

forming a conformal passivation layer on the gate insulation layer, the second conductive layer, the TFT structure, the data line and the gate line;

forming a first via hole penetrating the passivation layer to expose the surface of the source electrode;

forming a planarization layer on the passivation layer and filling the first via hole;

forming a second via hole and a third via hole penetrating the planarization layer, wherein the second via hole exposes at least the surface of the source electrode, and the third via hole exposes the surface of the passivation layer in the capacitor area; and

forming a conformal third conductive layer on part of the planarization layer and electrically connecting the source electrode;

wherein a storage capacitor structure is composed of the second conductive layer, the passivation layer and the third conductive layer in the capacitor area.

B. Claims 1 –13 are cancelled.

Allowed Subject Matter

3. Claims 14 – 26 are allowed.

4. The following is a statement of reasons for allowance.

Zhong et al. (US 6,060,714) teaches an X- ray imager including a thin film transistor comprising the steps of: providing a substrate having a capacitor area and a transistor area; forming a conformal gate insulation layer and a conformal dielectric layer on the gate electrode and the substrate; forming a semiconducting island on the gate dielectric layer in the transistor area; forming a source electrode and a drain electrode on the semiconducting island to form a thin film transistor (TFT) structure; forming a first conductive layer on the gate insulation layer in the capacitor area; forming a conformal dielectric layer on the first conductive layer in the capacitor area; forming a first planarization layer over the transistor and capacitor areas; forming a first, second and third hole in the first planarization layer; forming a conformal conductive layer the patterned first planarization layer and electrically connecting the source electrode; wherein a storage capacitor structure is composed of the first conductive layer, the dielectric layer and the conformal conductive layer in the capacitor area; and forming a second planarization film over the conformal conductive layer.

The prior art does not teach or suggest incombination with the other claimed limitations, a method comprising: forming a first conductive layer on the semiconducting layer; using a gray-tone photolithography, removing part of the

first conductive layer and the semiconducting layer to form a common line longitudinally extending on a first semiconducting island, and a source electrode, a drain electrode and a longitudinally extending data line on a second semiconducting island thereby forming a thin film transistor (TFT) structure, wherein the drain electrode electrically connects the data line; forming a second conductive layer on the gate insulation layer in the capacitor area and to cover the common line; forming a conformal passivation layer on the gate insulation layer, the second conductive layer, the TFT structure, the data line and the gate line; forming a first via hole penetrating the passivation layer to expose the surface of the source electrode; forming a planarization layer on the passivation layer and filling the first via hole; forming a second via hole and a third via hole penetrating the planarization layer, wherein the second via hole exposes at least the surface of the source electrode, and the third via hole exposes the surface of the passivation layer in the capacitor area; and forming a conformal third conductive layer on part of the planarization layer and electrically connecting the source electrode; wherein a storage capacitor structure is composed of the second conductive layer, the passivation layer and the third conductive layer in the capacitor area.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ikeda et al. (US 6,323,490) teaches an X-ray semiconductor detector.

Rostoker et al. (US 5,688,709) teaches a method for forming composite trench- fin capacitors.

Harari et al. (US 4,612,629) teaches a highly scalable ram cell.

Han et al. (US 6,521,924) teaches an image sensor incorporating a capacitor structure.

Lepert et al. (US 6,440,814) teaches an electrostatic discharge protector for sensors.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl White, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public

PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2813

August 5, 2004

C. Chaudhari

Chandra Chaudhari
Primary Examiner